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Reg. No. : .....

Name : .....

Fourth Semester B.Tech. Degree Examination, February 2015
(2008 Scheme)
Branch : Computer Science
08.403 : COMPUTER HARDWARE DESIGN (R)
(Special Supplementary)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **(10×4= 40 Marks)**

1. Explain how non-restoring algorithm gives better performance than restoring algorithm ?
2. Draw the schematic for 2×2 bit array multiplier.
3. Explain normalization of floating-point data with an example.
4. Design a circuit to implement following micro-operations.

   T_3 : if (c=0) then a ← a+b

   else if (d = 1) then a ← a+c
5. Show how arithmetic shift left operation differ in 2's complement, 1's complement and signed-magnitude representations.
6. What is scratch-pad memory ? Explain its benefits.
7. Explain about micro-program.
8. Write a short note on micro-program sequences.
9. What is the difference between PLA control and ROM control ?
10. Explain the advantages of sequence register and decoder method over one flip-flop per state method.

P.T.O.

PART – B

MODULE – I

11. a) Explain with example how divide overflow can be detected. 5

    b) Using restoring division method divide –125 by +18. 15

OR

12. a) Using Booth's method find the value of binary pattern $(11101110011)_2$. 6

    b) With the help of flow chart explain floating point addition-subtraction algorithm. 14

MODULE – II

13. Show the full designing steps of an accumulator and draw its one typical stage ? 20

OR

14. a) What is the range of numbers that can be accommodated in a 16-bit register when the binary numbers are represented in

    a) sign-magnitude

    b) sign-2's complement

    Give the answers in equivalent decimal representation. 10

    b) Explain bus organization inside CPU. 10

MODULE – III

15. a) Explain micro-programmed CPU organization. 15

    b) Compare horizontal and vertical micro instructions. 5

OR

16. Give the design of hard wired control for binary multiplier. 20